ABSTRACT

In a memory array structured of memory cells using a storage circuit STC and a comparator CP, either one electrode of a source electrode or a drain electrode of a transistor, whose gate electrode is connected to a search line, of a plurality of transistors structuring the comparator CP is connected to a match line HMLr precharged to a high voltage. Further, a match detector MDr is arranged on a match line LMLr precharged to a low voltage to discriminate a comparison signal voltage generated at the match line according to the comparison result of data. According to such memory array structure and operation, comparison operation can be performed at low power and at high speed while influence of search-line noise is avoided in a match line pair. Therefore, a low power content addressable memory which allows search operation at high speed can be realized.